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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/066,444	02/05/2002	Eric Lenormand	219177US2	2210
22850	7590	02/23/2006	EXAMINER	
OBLON, SPIVAK, MCCLELLAND, MAIER & NEUSTADT, P.C.			ALHIJA, SAIF A	
1940 DUKE STREET			ART UNIT	
ALEXANDRIA, VA 22314			PAPER NUMBER	
			2128	

DATE MAILED: 02/23/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

10/066,444

Applicant(s)

LENORMAND, ERIC

Examiner

Saif A. Alhija

Art Unit

2128

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 05 February 2002.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-8 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-8 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 05 February 2002 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date 4/22/02.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

**DETAILED ACTION**

1. Claims 1-8 have been presented for examination.

**PRIORITY**

2. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d).

**Information Disclosure Statement**

3. The information disclosure statement (IDS) submitted on 22 April 2002 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the Examiner has considered the IDS as to the merits.

**Specification Objections**

4. The specification and abstract are replete with numerous misspellings and errors. A substitute specification as well as claims is required pursuant to 37 CFR 1.125(a) because of the numerous spelling errors.

A substitute specification must not contain new matter. The substitute specification must be submitted with markings showing all the changes relative to the immediate prior version of the specification of record. The text of any added subject matter must be shown by underlining the added text. The text of any deleted matter must be shown by strike-through except that double brackets placed before and after the deleted characters may be used to show deletion of five or fewer consecutive characters. The text of any deleted subject matter must be shown by being placed within double brackets if strike-through cannot be easily perceived. An accompanying clean version (without markings) and a statement that the substitute specification contains no new matter must also be supplied. Numbering the paragraphs of the specification of record is not considered a change that must be shown.

5. With regards to paragraph 104 of the instant application, the invention is restricted to the claimed invention.

**Claim Objections**

6. **Claims 1-8 are objected** to because of the following informalities:

Claim 1 contains a misspelling of the word “following”.

Claim 1 contains the number 10 between “target architecture.” This appears to be a reference identifier, which does not appear to be in the specification.

Claim 2 contains the misspelling of the word “list”, “determine”, and “services”.

Claim 3 contains the letter t after claim 2.

Claim 7 contains the misspelling of the word “model”.

Claim 8 contains the misspelling of the word “to”.

Claim 8 contains the phrase “means of” which should be replaced with the phrase “means for”.

The examples above are exemplary of the types of objections present in the Claims. Appropriate correction is required.

7. **Claim 5 is objected** to under 37 CFR 1.75(c) as being in improper form because a multiple dependent claim cannot depend on another multiple dependent claim. See MPEP § 608.01(n). Accordingly, the claim has not been further treated on the merits.

**Claim Interpretation**

8. The Claims contain reference identifiers, which appear to be means for/steps for identifiers. It this is not Applicants intent please remove all instances of these identifiers.

The Claims are difficult to follow due to numerous misspellings therefore a new set of claims is required, as noted earlier.

The Claims are interpreted to be a simulation of a multiprocessor application that utilizes tasks, hardware, and software.

**Claim Rejections - 35 USC § 101**

35 U.S.C. 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

9. **Claims 1-8 are rejected** under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

It appears that the claims recite a computer program, although the word “device” for example may be used, and are therefore non-statutory. It should be noted that code (i.e., a computer software program) does not do anything per se. Instead, it is the code stored on a computer that, *when executed*, instructs the computer to perform various functions. The following claim is a generic example of a proper computer program product claim;

A computer program product embodied on a computer-readable medium and comprising code that, when executed, causes a computer to perform the following:

Function A  
Function B  
Function C, etc...

**Claim Rejections - 35 USC § 112**

**The following is a quotation of the first paragraph of 35 U.S.C. 112:**

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

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10. **Claim 8 is rejected** under 35 U.S.C. 112, first paragraph, for undue breadth. The claim contains a single means and is therefore nonenabling for the scope of the claim because the specification disclosed at most only those means known to the inventor. See MPEP 2164.08(a).

**Claim Rejections - 35 USC § 102**

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

11. **Claims 1-4, 6-8 are rejected** under 35 U.S.C. 102(b) as being clearly anticipated by **Applicants own Background and Description of Prior Art.**

**Regarding Claim 1:**

**Applicant discloses** Process for simulating a multiprocessor application placed on a target architecture, characterized in that it includes at least the following steps:

(a) a step (E2) to prepare the simulation to produce a services graph (D3), using firstly a tasks graph (D2) and secondly a list of mechanisms and their definition (A2); **(Page 1, Paragraphs 1 and 2)**

(b) a step (E3) to execute the simulation to determine the performance of the placed application, using a behavioral model (A3) of the target 10 architecture and the services graph (D3). **(Page 1,**

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**Paragraphs 1 and 2)**

**Regarding Claim 2:**

**Applicant discloses** Process for producing a multiprocessor application, characterized in that it includes at least the following steps:

(a) a step (E1) to place the application on the target architecture using firstly a functional description (D1) of said application, and secondly the list of resources (A1) of the target architecture in order to produce a tasks graph (D2); **(Page 1, Paragraphs 1 and 2)**

(b) a step (E2) to prepare a simulation to produce a services graph (D3) starting firstly from a tasks graph (D2), and secondly from a list of mechanisms and their definitions (A2); **(Page 1,**

**Paragraphs 1 and 2)**

(c) a step (E3) to execute the simulation to determine the performance of the placed application, using a behavioral model (A3) of the target architecture and the services graph (D3). **(Page 1,**

**Paragraphs 1 and 2)**

**Regarding Claim 3:**

**Applicant discloses** Process according to claim 2, characterized in that said placement step (E1) includes a partitioning step (P1) and a mapping step (P2). **(Page 1, Paragraphs 3 and 4)**

**Regarding Claim 4:**

**Applicant discloses** Process according to any of the previous claims, characterized in that said simulation preparation step (E2) includes a step to create objects representing services, these objects being created by objects representing mechanisms. **(Page 1, Paragraphs 1 and 2)**

**Regarding Claim 6:**

**Applicant discloses** Device used to create a multiprocessor application, characterized in that it includes;

(a) a placement aid (G1) that a mapper can use to place a functionally described application on a target architecture, **(Page 1, Paragraphs 5 and 6)**

(b) an architecture model (A3) including behavioral models of elements of the architecture; **(Page 1, Paragraphs 1 and 2)**

(c) a simulation engine (G2), using the architecture model to determine the performance of the placed application. **(Page 1, Paragraphs 1 and 2)**

**Regarding Claim 7:**

**Applicant discloses** Device according to claim 6, characterized in that said architecture model (A3) includes a generic interface independent of the target architecture that can be modified when the target architecture is modified, without modifying the placement aid (G1) and without modifying the simulation engine (G2). **(Page 1, Paragraphs 7 and 8)**

**Regarding Claim 8:**

**Applicant discloses** Device according to claim 6, characterized in that it includes means of reading firstly said list of resources (A1) of the target architecture, and secondly said list of mechanisms and their definitions (A2). **(Page 1, Paragraphs 1 and 2)**

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**12. Claims 1-4, 6-8 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Chan “Multithreaded, Mixed Hardware Description Languages Logic Simulation on Engineering Workstations”, U.S. Patent No. 6,466,898, hereafter referred to as Chan.**

**Regarding Claim 1:**

**Chan discloses** Process for simulating a multiprocessor application placed on a target architecture, characterized in that it includes at least the following steps:

(a) a step (E2) to prepare the simulation to produce a services graph (D3), using firstly a tasks graph (D2) and secondly a list of mechanisms and their definition (A2); **(Column 1, Lines 20-30.**

**Figures 4 and 5)**

(b) a step (E3) to execute the simulation to determine the performance of the placed application, using a behavioral model (A3) of the target 10 architecture and the services graph (D3). **(Column 1, Lines 7-30. Figures 4 and 5)**

**Regarding Claim 2:**

**Chan discloses** Process for producing a multiprocessor application, characterized in that it includes at least the following steps:

(a) a step (E1) to place the application on the target architecture using firstly a functional description (D1) of said application, and secondly the list of resources (A1) of the target architecture in order to produce a tasks graph (D2); **(Column 1, Lines 7-30. Figures 3, 4 and 5)**

(b) a step (E2) to prepare a simulation to produce a services graph (D3) starting firstly from a tasks graph (D2), and secondly from a list of mechanisms and their definitions (A2); **(Column 1, Lines 7-30. Figures 3, 4 and 5)**

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(c) a step (E3) to execute the simulation to determine the performance of the placed application, using a behavioral model (A3) of the target architecture and the services graph (D3). **(Column 1, Lines 7-30. Figures 3, 4 and 5)**

**Regarding Claim 3:**

**Chan discloses** Process according to claim 2, characterized in that said placement step (E1) includes a partitioning step (P1) and a mapping step (P2). **(Column 9, Lines 25-38. Figure 9)**

**Regarding Claim 4:**

**Chan discloses** Process according to any of the previous claims, characterized in that said simulation preparation step (E2) includes a step to create objects representing services, these objects being created by objects representing mechanisms. **(Column 2, Lines 23-37)**

**Regarding Claim 6:**

**Chan discloses** Device used to create a multiprocessor application, characterized in that it includes;

(a) a placement aid (G1) that a mapper can use to place a functionally described application on a target architecture, **(Column 1, Lines 7-30. Figures 3, 4 and 5)**

(b) an architecture model (A3) including behavioral models of elements of the architecture; **(Column 1, Lines 46-57)**

(c) a simulation engine (G2), using the architecture model to determine the performance of the placed application. **(Column 1, Lines 46-57)**

**Regarding Claim 7:**

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**Chan discloses** Device according to claim 6, characterized in that said architecture model (A3) includes a generic interface independent of the target architecture that can be modified when the target architecture is modified, without modifying the placement aid (G1) and without modifying the simulation engine (G2). (Column 10, Lines 15-21)

**Regarding Claim 8:**

**Chan discloses** Device according to claim 6, characterized in that it includes means of reading firstly said list of resources (A1) of the target architecture, and secondly said list of mechanisms and their definitions (A2). (Column 2, Lines 23-37)

**Conclusion**

13. All Claims are rejected.

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Saif A. Alhija whose telephone number is (571) 272-8635. The examiner can normally be reached on M-F, 11:00-7:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamini Shah can be reached on (571) 272-2279. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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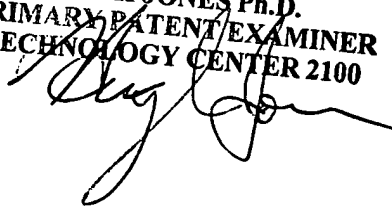
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SAA

February 20, 2006

HUGH JONES Ph.D.  
PRIMARY PATENT EXAMINER  
TECHNOLOGY CENTER 2100

A handwritten signature in black ink, appearing to read "Hugh Jones", is written over the printed name and title.